

DATA SHEET

PCA9559

5-bit multiplexed/1-bit latched 6-bit I²C
EEPROM

Product specification
Supersedes data of 1999 Oct 20

2000 Jan 31

5-bit multiplexed/1-bit latched 6-bit I²C EEPROM

PCA9559

FEATURES

- 5-bit 2-to-1 multiplexer, 1-bit latch
- 6-bit internal non-volatile register
- Internal non-volatile register programmable and readable via I²C bus
- Override input forces all outputs to logic 0
- 5 open drain multiplexed outputs
- 1 open drain non-multiplexed (latched) output
- 5V and 2.5V tolerant inputs
- Useful for ‘jumperless’ configuration of PC motherboards
- 2 address pins, allowing up to 4 devices on the I²C bus

DESCRIPTION

The primary function of the 5-bit multiplexer, 1-bit latch is to enable system configuration.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic TSSOP	0°C to +70°C	PCA9559 PW DH	SOT360-1

FUNCTIONAL DESCRIPTION

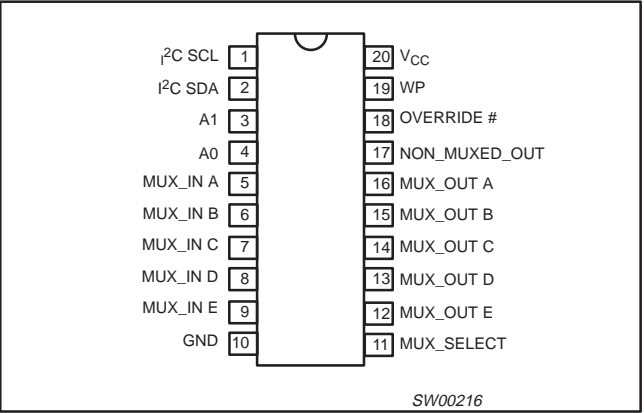
When the MUX_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX_OUT pins. When the MUX_SELECT signal is logic 1, the multiplexer will select the MUX_IN lines to drive on the MUX_OUT pins. The MUX_SELECT signal is also used to latch the NON_MUXED_OUT signal which outputs data from the non-volatile register. The NON_MUXED_OUT signal latch is transparent when MUX_SELECT is in a logic 0 state, and will latch data when MUX_SELECT is in a logic 1 state. When the active-LOW OVERRIDE# signal is set to logic 0 and the MUX_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1.

The Write Protect (WP) input is used to control the ability to write the contents of the 6-bit non-volatile register. If the WP signal is logic 0, the I²C bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I²C bus (described in the next section).

The OVERRIDE#, WP, MUX_IN, and MUX_SELECT signals have internal pullup resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

PIN CONFIGURATION



FUNCTION TABLE

OVERRIDE#	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0's	All 0's
0	1	MUX_IN inputs	Latched NON_MUXED_OUT 1
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

NOTE:
1. NON_MUXED_OUT state will be the value present on the output at the time of the MUX_SELECT input transitioned from a logic 0 to a logic 1 state.

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	I ² C SCL	Serial I ² C bus clock
2	I ² C SDA	Serial bi-directional I ² C bus data
3	A1 Address	A1
4	A0 Address	A0
5	MUX_IN A	External inputs to multiplexer
6	MUX_IN B	
7	MUX_IN C	
8	MUX_IN D	
9	MUX_IN E	
10	GND	Ground
11	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
12	MUX_OUT E	Open drain multiplexed outputs
13	MUX_OUT D	
14	MUX_OUT C	
15	MUX_OUT B	
16	MUX_OUT A	
17	NON_MUXED_OUT	Open drain outputs from non-volatile memory
18	OVERRIDE#	Forces all outputs to logic 0
19	WP	Non-volatile register write-protect
20	V _{CC}	Positive voltage rail

I²C INTERFACE

Communicating with this device is initiated by sending a valid address on the I²C bus. The address format (see Figure 1) has 5 fixed bits and two user-programmable bits followed by a 1-bit read/write value which determines the direction of the data transfer.

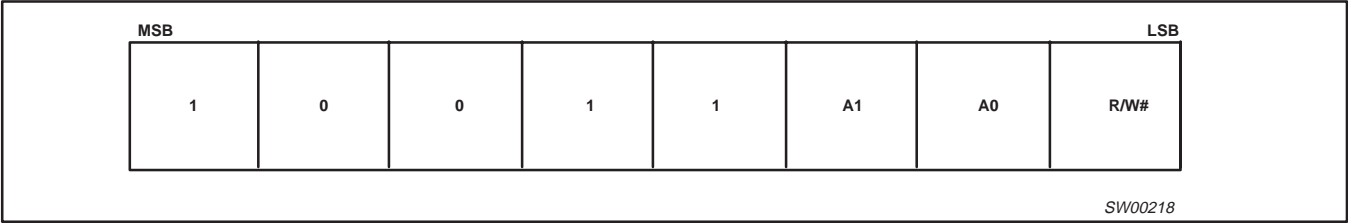


Figure 1. I²C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The four high-order bits are latched outputs, while the four low order bits are multiplexed outputs (Figure 2).

NOTE:

1. To ensure data integrity, the non-volatile register must be internally write protected when V_{CC} to the I²C bus is powered down or V_{CC} to the component is dropped below normal operating levels.

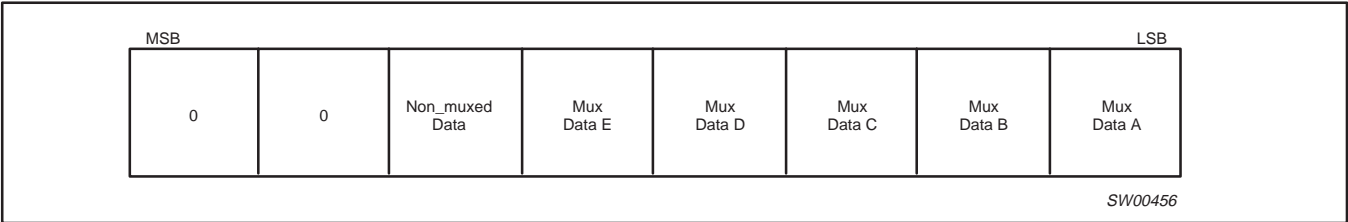
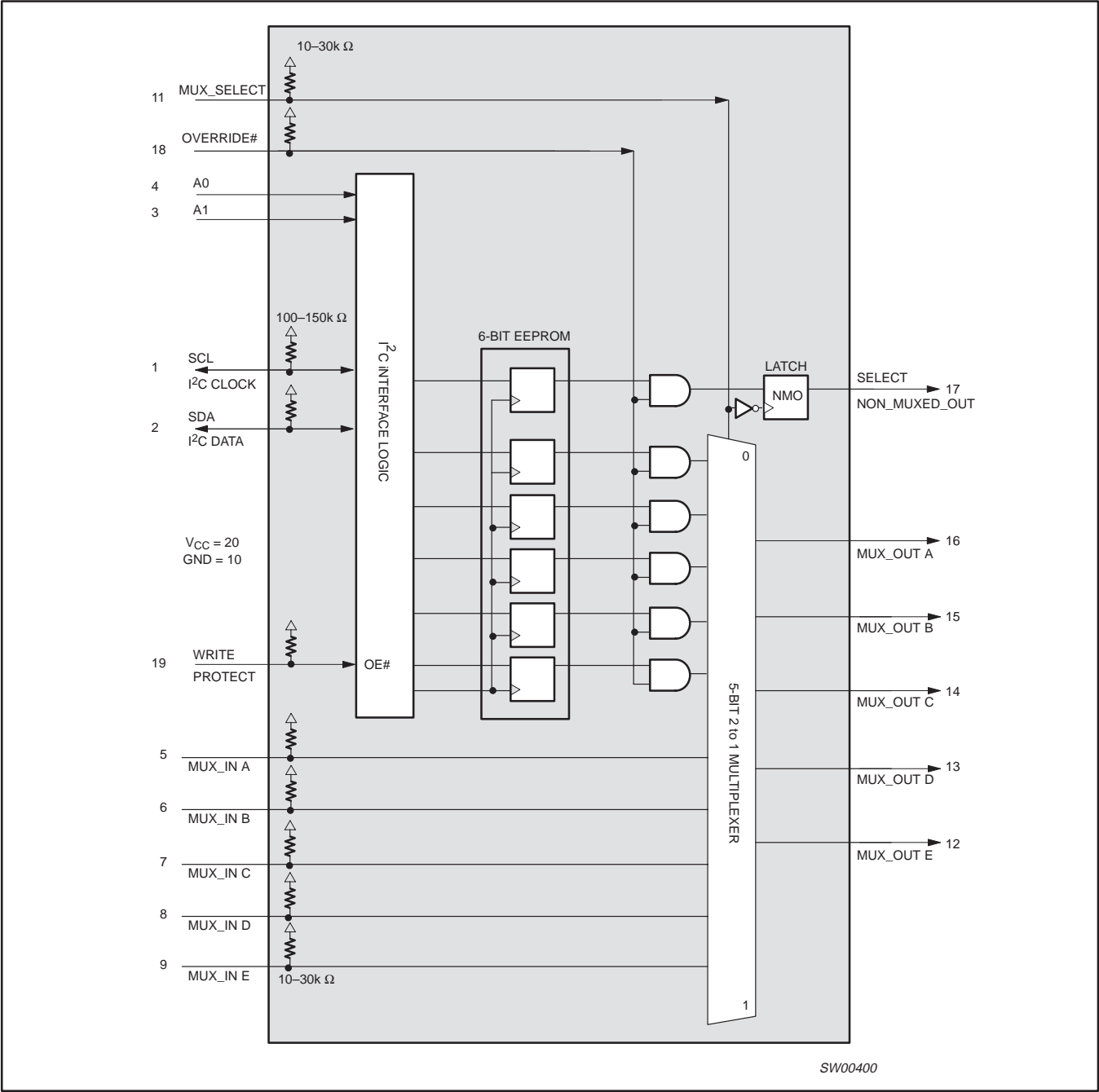


Figure 2. I²C Data Byte

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +4.6	V
V _I	DC input voltage	Note 3	−1.5 to V _{CC} +1.5	V
V _{OUT}	DC output voltage	Note 3	−0.5 to V _{CC} +0.5	V
T _{stg}	Storage temperature range		−60 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage		3.0	3.6	V
SCL, SDA	V _{IL}	I _{OL} = 3 mA	−0.5	0.9	V
	V _{IH}	I _{OL} = 3 mA	2.7	4.0	V
	V _{OL}	I _{OL} = 3 mA		0.4	V
	V _{OL}	I _{OL} = 6 mA		0.6	V
OVERRIDE#, MUX_IN, MUX_SELECT	V _{IL}		−0.5	0.8	V
	V _{IH}		2.0	4.0	V
MUX_OUT, NON_MUXED_OUT	I _{OL}			8	mA
	I _{OH}			100	μA
dt/dv	Input transition rise or fall time		0	10	ns/V
T _{amb}	Operating temperature		0	70	°C

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DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Supply						
V _{CC}	Supply Voltage		3		3.8	V
I _{CCL}	Supply Current	Operating mode ALL inputs = 0 V			10	mA
I _{CCH}	Supply Current	Operating mode ALL inputs = V _{CC}			600	μA
Input SCL: Input/Output SDA						
V _{IL}	Low Level Input Voltage		−0.5		0.8	V
V _{IH}	High Level Input Voltage		2		V _{CC} + 0.5	V
I _{OL}	Low Level Output Current	V _{OL} = 0.4	3			mA
I _{OL}	Low Level Output Current	V _{OL} = 0.6	6			mA
I _{IH}	Leakage Current High	V _I = V _{CC}	−1.5		−12	μA
I _{IL}	Leakage Current Low	V _I = GND	−7		−32	μA
C _I	Input Capacitance				10	pF
Override #, WP, Mux_Select						
I _{IH}	Leakage Current High	V _I = V _{CC}	−20		−100	μA
I _{IL}	Leakage Current Low	V _I = GND	−86		−267	μA
C _I	Input Capacitance				10	pF
Mux A → E						
I _{IH}	Leakage Current High	V _I = V _{CC}	−0.166		−0.75	mA
I _{IL}	Leakage Current Low	V _I = GND	−0.72		−2	mA
C _I	Input Capacitance				10	pF
A0, A1 Inputs						
I _{IH}	Leakage Current High	V _I = V _{CC}	−1		1	μA
I _{IL}	Leakage Current Low	V _I = GND	−1		1	μA
C _I	Input Capacitance				10	pF
Mux_Outputs						
V _{OL}	Low Level Output Current	(I _{OL} = 100 μA)			0.4	V
V _{OL}	Low Level Output Current	(I _{OL} = 2 mA)			0.7	V
Non_Mux_Output						
V _{OL}		(I _{OL} = 100 μA)			0.4	V
V _{OL}		(I _{OL} = 2 mA)			0.7	V

NOTES:

1. V_{HYS} is the hysteresis of Schmitt-Trigger inputs

NON-VOLATILE STORAGE SPECIFICATIONS

PARAMETER	SPECIFICATION
Memory cell data retention	10 years min
Number of memory cell write cycles	3,000 cycles min

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AC CHARACTERISTICS

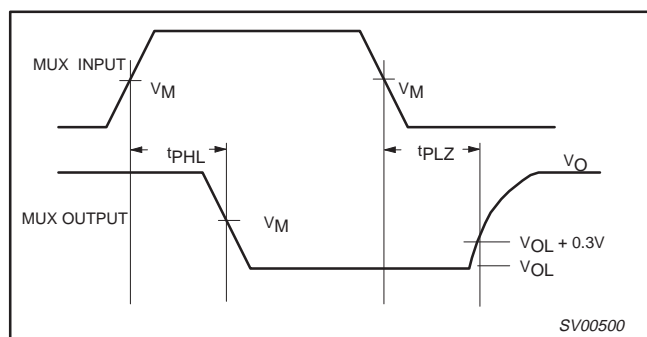
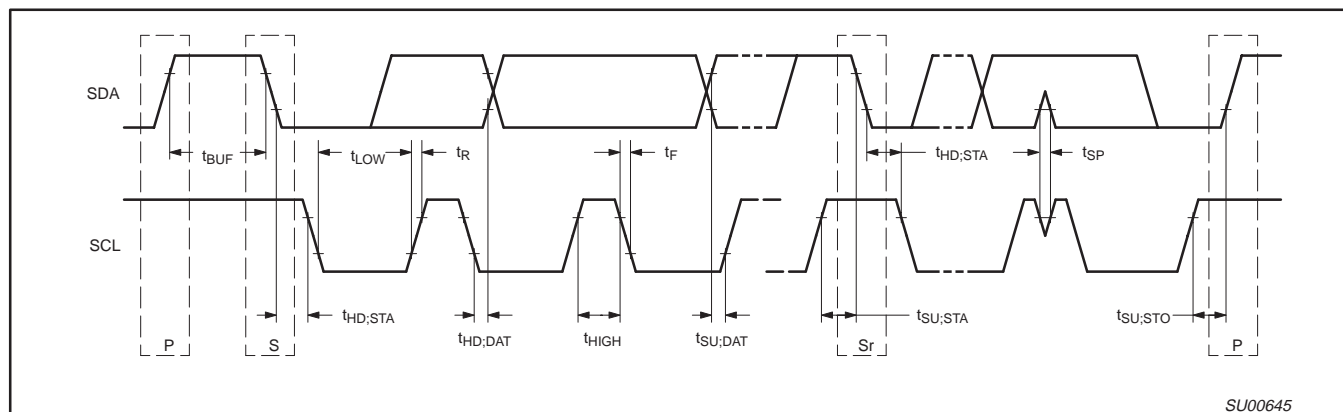
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
MUX_in ⇒ MUX_out					
T _{plh}			28	37	nS
T _{phl}			16	21	nS
Select ⇒ MUX_out					
T _{plh}			30	39	nS
T _{phl}			17	22	nS
Override ⇒ Non-MUX_out					
T _{plh}			34	43	nS
T _{phl}			19	25	nS
Override ⇒ MUX_out					
T _{plh}			31	41	nS
T _{phl}			21	27	nS
T _R	Output rise time	1.0		3	ns/V
T _F	Output fall time	1.0		3	ns/V
P _F	Pull-up resistor for outputs	1.0			ns/V
C _L	Test load capacitance on outputs				pF
I ² C Bus					
t _{SCL}	SCL clock frequency	10		400	kHz
t _{BUF}	Bus free time between a STOP and a START condition	1.3			μs
t _{HD:STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	600			ns
t _{LOW}	LOW period of SCL clock	1.3			μs
t _{HIGH}	HIGH period of SCL clock	600		−12	ns
t _{SU:STA}	Set-up time for a repeated START condition	600		−32	ns
t _{HD:DAT}	Data hold time	0		10	ns
t _{SU:DAT}	Data set-up time	100		−100	ns
t _{SP}	Data spike time	0		50	ns
t _{SU:STO}	Set-up time for STOP condition	600		10	ns
t _R	Rise time for both SDA and SCL signals (10 – 400 pF bus)	20		300	ns
t _I	Fall time for both SDA and SCL signals (10 – 400 pF bus)	20		300	ns
C _L	Capacitive load for each bus line			400	pF
T _W	Write cycle time ¹		15		mS

NOTE:

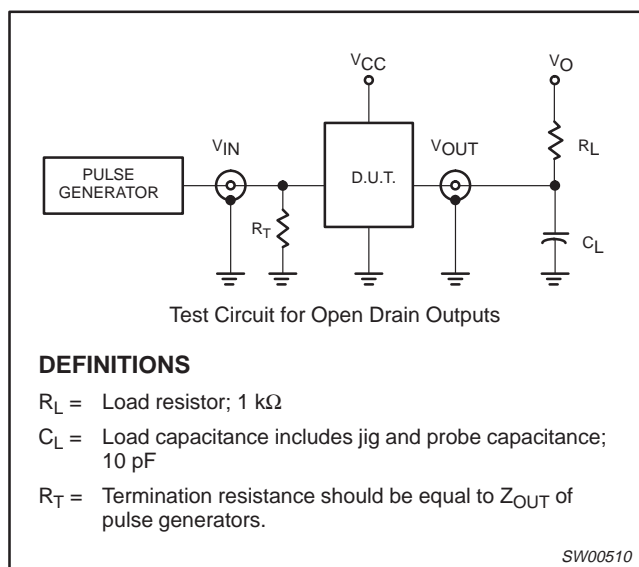
1. WRITE CYCLE time can only be measured indirectly during the write cycle. During this time, the device will not acknowledge its I²C Address.

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Waveform 1. Open drain output enable and disable times

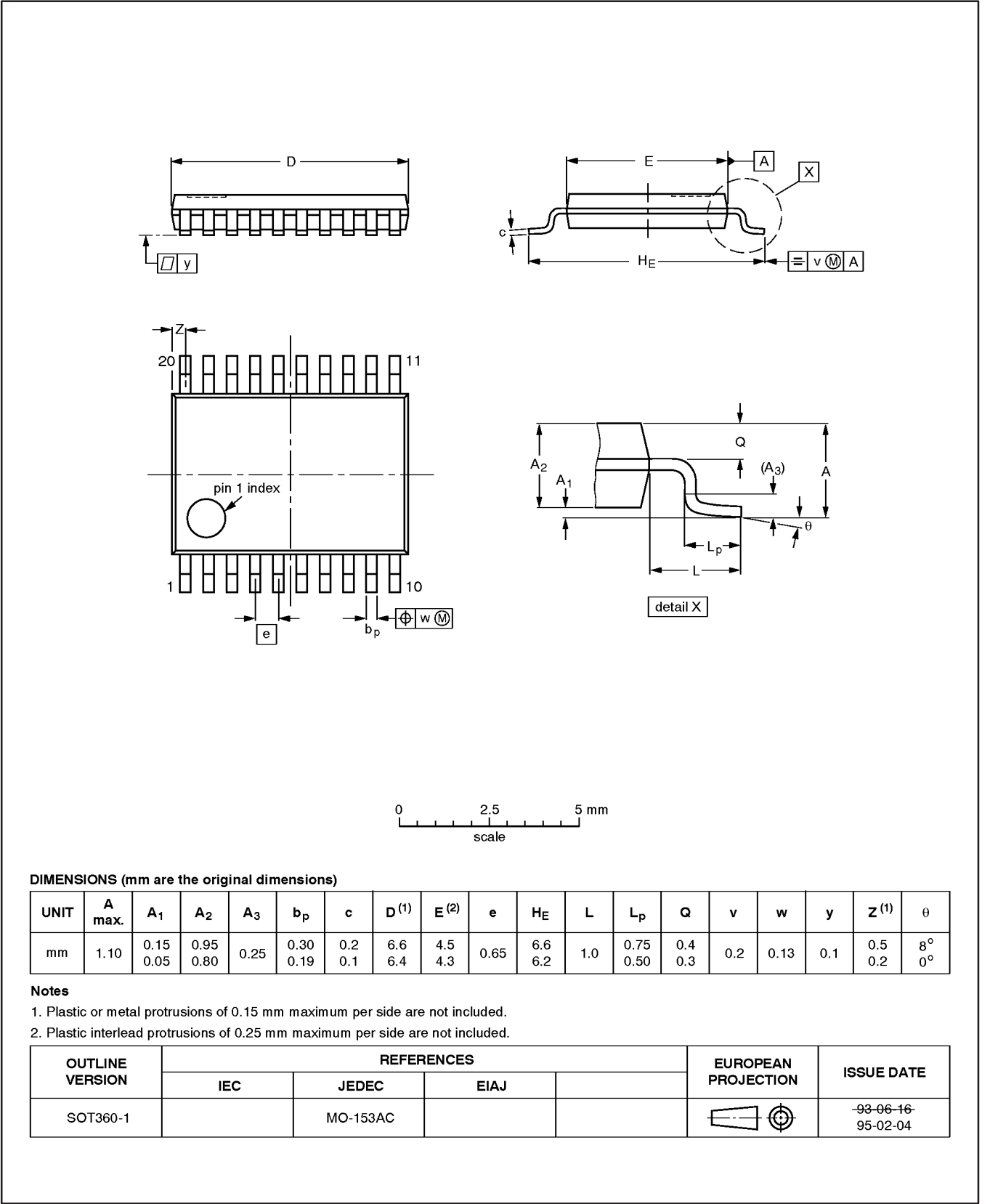


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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